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A Hartstein, TR Puzak - Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual ..., 2003 - [ieeexplore.ieee.org](#)

... using IPC degradation factors for adding **cycles** to critical ... **power** be just below some **maximum** value, which ... detailed comparisons of theory and **simulation** for all ...

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Advances in modeling and simulation of vacuum electronic devices - group of 4 »

TM Antonsen Jr, AA Mondelli, B Levush, JP ... - Proceedings of the IEEE, 1999 - [ieeexplore.ieee.org](#)

... the design to be realized with fewer test **cycles**. ... designing and optimizing the interaction **circuit**, the electron gun ... et al.: ADVANCES IN MODELING AND **SIMULATION** ...

Cited by 22 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

The optimum pipeline depth considering both power and performance

A Hartstein, TR Puzak - ACM Transactions on Architecture and Code Optimization (TACO) ..., 2004 - [portal.acm.org](#)

... that the **power** be just below some **maximum** value, which ... to perform detailed comparisons

of theory and **simulation** for all ... where the **cycle** time, t_s , is split up ...

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A Two-Dimensional Multispecies Fluid Model of the Plasma in an AC Plasma

Display Panel - group of 3 »

RB Campbell, R Veerasingham, RT McGrath - IEEE TRANSACTIONS ON PLASMA SCIENCE, 1995 - [ieeexplore.ieee.org](#)

... the orderings can change during the discharge **cycle**. ... the surface charge density, external **circuit**, and electrostatic ... of the computation time in any **simulation**. ...

Cited by 33 - [Related Articles](#) - [Web Search](#)

[PS] A Microarchitecture for High-speed, Resource-limited, Superscalar Microprocessor

TD Basso - [eecs.umich.edu](#)

... driven **simulation** of the Spec95 integer benchmark suite will be ... be mounted on a printed

circuit board configured ... are attempting to exploit the **maximum**, or **peak** ...

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POWER ESTIMATION AND POWER OPTIMIZATION POLICIES FOR PROCESSOR-BASED SYSTEMS

JLA Rodrigo - [lsi.die.upm.es](#)

... the registers while reducing the **power** consumption to a **minimum**. ... the general trend is for **maximum** processor **power** ... due to the lack of **simulation** information at ...

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A Cell-Sparing Electric Field Stimulation Technique for High-Throughput

Screening of Voltage-Gated ... - group of 3 »

RM Bugianesi, PR Augustine, K Azer, C Dufresne, J ... - ASSAY and Drug Development Technologies, 2006 - liebertonline.com

... The **simulation** is with 1 V applied via the non ... This **circuit** was configured as an "Improved Howland Current Pump ... frequency of 0.5–100 Hz for 1–1000 **cycles**. ...

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A new CCD designed for curvature wavefront sensing - group of 2 »

JW Beletic, RJ Dorn, T Craven-Bartle, B Burke - Optical Detectors for Astronomy II, Kluwer Academic ..., 2000 - eso.org

... **Simulation** parameters: 0.66 arc sec seeing (at 500 nm ... If the **maximum** amplitude of the membrane vibration is ... kHz membrane frequency with the **minimum** focal length ...

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[book] The Designer's Guide to High-Purity Oscillators - group of 2 »

EE Hegazi, J Rael, AA Abidi - 2004 - books.google.com

... 11.2 Device Limitations on **Maximum** Swing ... utilized yet we tried to keep that to the **minimum** necessary. ... [2] KS Kundert, "Introduction to RF **simulation** and its ...

[Cited by 4](#) - [Related Articles](#) - [Web Search](#) - [Library Search](#)

REAL-TIME SENSING OF FATIGUE CRACK DAMAGE FOR INFORMATION-BASED DECISION AND CONTROL

E Keller - 2001 - etda.libraries.psu.edu

... Figure 3-7 **Peak** value of ultrasonic signal Specimen Sk. ... 35 Time in units of 200 **cycles** ...

demonstrated by **simulation** the benefits of an optimal open loop control ...

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Simulation and optimization of the power distribution network in VLSI circuits
 - group of 9 »

 G Bai, S Bobba, IN Hajj... - Proc. International Conference on Computer-Aided Design, 2000
 - doi.ieeecomputersociety.org

 ... sensitivity based decoupling capacitance optimization for this **circuit**. ... a node by
 time-domain **simulation** of the ... cell for different number of **cycles** using the ...

 Cited by 35 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)
Microarchitectural simulation and control of di/dt-induced power supply
voltage variation - group of 7 »

 E Grochowski, D Ayers, V Tiwari - High-Performance Computer Architecture, 2002.
 Proceedings. ..., 2002 - ieeexplore.ieee.org

 ... MHz) components caused by the **circuit** board, connector ... distribution network
 (approximately 25 clock **cycles** in figure 2 ... algorithm used by the **simulator** to compute ...

 Cited by 21 - [Related Articles](#) - [Web Search](#)
Power-aware microarchitecture: design and modeling challenges for next-
generation microprocessors - group of 14 »

 DM Brooks, P Bose, SE Schuster, H Jacobson, PN ... - Micro, IEEE, 2000 -
 ieeexplore.ieee.org

 ... that we can use clock-gating techniques at the **circuit** level (for exam ... of the key
 functional units, based on a detailed, **cycle**-accurate **simulation** of a ...

 Cited by 117 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)
Electrothermal simulation of an IGBT PWM inverter - group of 4 »

 HA Mantooh, AR Hefner Jr, A Inc, OR Beaverton - Power Electronics, IEEE Transactions
 on, 1997 - ieeexplore.ieee.org

 ... the dissipated **power** over a complete 60-Hz **cycle**. ... condition for another full
 electrothermal **simulation** in Step 1 ... were required for this **circuit** to determine ...

 Cited by 21 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)
Power-sensitive multithreaded architecture - group of 10 »

 JS Seng, DM Tullsen, GZN Cai - International Conference on Computer Design, 2000 -
 doi.ieeeecs.org

 ... coarse assumption that the general **circuit** makeup of ... threshold values are fixed
 throughout a given **simulation**. ... threads that are selected each **cycle** to attempt ...

 Cited by 60 - [Related Articles](#) - [Web Search](#)
Adaptive piezoelectric energy harvesting circuit for wireless remote power
supply - group of 3 »

 GK Ottman, HF Hofmann, AC Bhatt, GA Lesieutre - Power Electronics, IEEE Transactions
 on, 2002 - ieeexplore.ieee.org

 ... controller allows the energy harvesting **circuit** to be ... the remainder of the half-**cycle**,
 the interval ... methods to the design and **simulation** of electromechanical ...

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... dynamic voltage scaling and adaptive body biasing for lower power
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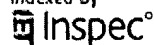
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Peak power tracking in parallel connected convertors

Siri, K. Caliskan, V.A. Lee, C.Q.
Electron. Res. Lab., Illinois Univ., Chicago, IL ;

This paper appears in: [Circuits, Devices and Systems, IEE Proceedings G](#)

Publication Date: Apr 1993

Volume: 140, Issue: 2

On page(s): 106-116

ISSN: 0956-3768

References Cited: 7

CODEN: IPGSEB

INSPEC Accession Number: 4397694

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Abstract

A control scheme for parallel connected convertor systems, which will transfer the maximum average power from a nonideal voltage source, is presented. Monitoring the rates of change in both the average and average input power from the source, the proposed control method can dynamically regulate the convertor system to track the peak power point of the source. The amplitude and frequency of the limit cycle around the system peak power point is analysed. To improve the system reliability, the central limit distribution control is incorporated into the proposed scheme to uniformly supplied power among the parallel connected convertors.

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IEEE JNL IEEE Journal or Magazine

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- ☐ 1. Application of genetically engineered finite-state-machine sequences to ATPG
Hsiao, M.S.; Rudnick, E.M.; Patel, J.H.;
[Computer-Aided Design of Integrated Circuits and Systems](#), IEEE Transaction:
Volume 17, Issue 3, March 1998 Page(s):239 - 254
Digital Object Identifier 10.1109/43.700722
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(368 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 2. Fast static compaction algorithms for sequential circuit test vectors
Hsiao, M.S.; Rudnick, E.M.; Patel, J.H.;
[Computers](#), IEEE Transactions on
Volume 48, Issue 3, March 1999 Page(s):311 - 322
Digital Object Identifier 10.1109/12.754997
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(484 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 3. Peak power estimation of VLSI circuits: new peak power measures
Hsiao, M.S.; Rudnick, E.M.; Patel, J.H.;
[Very Large Scale Integration \(VLSI\) Systems](#), IEEE Transactions on
Volume 8, Issue 4, Aug. 2000 Page(s):435 - 439
Digital Object Identifier 10.1109/92.863624
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(148 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 4. Partial scan selection based on dynamic reachability and observability in
Hsiao, M.S.; Saund, G.S.; Rudnick, E.M.; Patel, J.H.;
[VLSI Design, 1998. Proceedings., 1998 Eleventh International Conference on](#)
4-7 Jan. 1998 Page(s):174 - 180
Digital Object Identifier 10.1109/ICVD.1998.646598
[AbstractPlus](#) | Full Text: [PDF](#)(816 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 5. K2: an estimator for peak sustainable power of VLSI circuits
Hsiao, M.S.; Rudnick, E.M.; Patel, J.H.;
[Low Power Electronics and Design, 1997. Proceedings., 1997 International Sy](#)
18-20 Aug 1997 Page(s):178 - 183

[AbstractPlus](#) | Full Text: [PDF\(752 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ 6. **Sequential circuit test generation using dynamic state traversal**
Hsiao, M.S.; Rudnick, E.M.; Patel, J.H.;
[European Design and Test Conference, 1997. ED&TC 97. Proceedings](#)
17-20 March 1997 Page(s):22 - 28
Digital Object Identifier 10.1109/EDTC.1997.582325
[AbstractPlus](#) | Full Text: [PDF\(736 KB\)](#) IEEE CNF
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- ☐ 7. **Parallel genetic algorithms for simulation-based sequential circuit test ge**
Krishnaswamy, D.; Hsiao, M.S.; Saxena, V.; Rudnick, E.M.; Patel, J.H.; Banerj
[VLSI Design, 1997. Proceedings., Tenth International Conference on](#)
4-7 Jan. 1997 Page(s):475 - 481
Digital Object Identifier 10.1109/ICVD.1997.568180
[AbstractPlus](#) | Full Text: [PDF\(712 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ 8. **Effects of delay models on peak power estimation of VLSI sequential circ**
Hsiao, M.S.; Rudnick, E.M.; Patel, J.H.;
[Computer-Aided Design, 1997. Digest of Technical Papers., 1997 IEEE/ACM I](#)
[Conference on](#)
9-13 Nov. 1997 Page(s):45 - 51
Digital Object Identifier 10.1109/ICCAD.1997.643360
[AbstractPlus](#) | Full Text: [PDF\(768 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ 9. **Automatic test generation using genetically-engineered distinguishing se**
Hsiao, M.S.; Rudnick, E.M.; Patel, J.H.;
[VLSI Test Symposium, 1996., Proceedings of 14th](#)
28 April-1 May 1996 Page(s):216 - 223
Digital Object Identifier 10.1109/VTEST.1996.510860
[AbstractPlus](#) | Full Text: [PDF\(792 KB\)](#) IEEE CNF
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- ☐ 10. **Alternating strategies for sequential circuit ATPG**
Hsiao, M.S.; Rudnick, E.M.; Patel, J.H.;
[European Design and Test Conference, 1996. ED&TC 96. Proceedings](#)
11-14 March 1996 Page(s):368 - 374
Digital Object Identifier 10.1109/EDTC.1996.494327
[AbstractPlus](#) | Full Text: [PDF\(612 KB\)](#) IEEE CNF
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